Method and Apparatus for Independently Controlling Each Phase of a Multi-phase Step Motor

Background of the Invention

When operating a multi-phase step motor, the phase current to the motor must be accurately controlled to cause motor movement as well as to hold the motor position when stopped. The degree of control impacts stability while in motion and positional accuracy when stationary. One such method for controlling the operation of a stepper motor is described within US patent 5,264,770 entitled "Stepper Motor Driver Circuit". Other methods for controlling multi-phase step motors are found within US patent 5,650,705 entitled "Apparatus and Method for Controlling Currents in an Inductor" and US patent 6,049,184 entitled "Method and Arrangement for Controlling a Current".

Such methods often utilize a fixed frequency pulse width modulator "PWM" consisting of a single comparator for each phase to determine when the phase current is at or above a set point. However, when the motor is moving at high speed the condition of excess current caused by back electromotive force, "EMF", is difficult to determine such that the "PWM" frequency may not provide sufficient opportunity to control the motor current and there is no provision to stop the motor current based on a time factor.

One purpose of the present invention is to control the motor current independently in each motor phase of a multi-phase step motor to a set current value.

Summary of the Invention

The current in each phase of a multi-phase step motor is monitored and the excess phase current above the set point current, as required on a cycle-by-cycle PWM basis, is reduced thereby bringing each phase current down to the set point. The active

independent removal of excess phase current caused by back EMF allows accurate current control at higher motor operating speeds and reduces phase lag. The PWM frequency is automatically adjusted to maintain a minimum number of active edges within the specified upper frequency limit during the front slope portion of the current waveform when the step motor is in motion. Automatic adjustment of PWM frequency above the base frequency provides more accurate construction of the current waveform at higher motor speeds. A maximum charge / discharge time is specified as a percentage of the PWM period. Controlling the maximum charge and discharge time provides a further benefit as it can be used to compensate for extremes in system response caused by very low inductance motors and/or very high motor supply voltage. These provide accurate independent current control within each phase of a multiphase step motor.

Brief Description of the Drawings

Figure 1 is a diagrammatic representation of the step motor driver circuit in accordance with the teachings of the invention; and

Figure 2 is a diagrammatic representation of the PWM oscillator waveform and TEST waveform within the step motor driver circuit of Figure 1.

Description of the Preferred Embodiment

As shown in Figure 1, one motor phase coil 9 of a multiphase motor (not shown) is interconnected with the driver circuit 10 by means of an H bridge switch arrangement, hereafter "H bridge" 16 consisting of switches S1-S4, similar to that shown in the aforementioned US patent 6,049,184 for individual control of each separate motor phase. Although only one motor phase coil 9 is depicted, it is understood that the driver circuit 10 connects in a similar manner with the other motor phase coils (not shown).

By activating the appropriate switches S1-S4 current can be directed through the phase coil 9 in different directions. In accordance with the teachings of the invention, FORWARD CURRENT "FWD" is defined herein as increasing current away from zero. REVERSE CURRENT "REV" is defined as decreasing current toward zero. To achieve FWD current or REV current one switch in the upper portion and one switch in the lower portion of the H bridge are activated.

RECIRCULATING CURRENT "RECIRC" is defined as allowing current to move within the upper or lower portion of the H bridge 16 when FWD or REV current has been terminated. To achieve RECIRC current, both switches in the lower portion or both switches in the upper portion of the H bridge are activated. The signals that define the direction of current flow are SIGN and TEST.

In operation, a PWM oscillator 12 creates the TEST signal (item 37, Figure 2) onto conductor 21 and PWM_OSC signal (item 36, Figure 2) onto conductor 22 which direct the bridge control logic 14 to assert the appropriate switches S1-S4 in the H bridge 16. Phase current is sensed during FWD and REV across resistor R1 creating an I_SENSE signal on conductor 23 which is conditioned by signal conditioning circuit 24, consisting of paired op amps 17, 18 and then compared to the SET_POINT signal generated on conductor 25 by the set point generator 11, using the paired comparators 19, 20. The comparators 19, 20 create two signals, FWD on conductor 27, which indicates that FWD current is at or above the SET_POINT during the forward condition, and REV on conductor 28, which indicates that the REV current is at or above the SET_POINT during the reverse condition

The set point generator 11 provides the SIGN signal on conductor 26, SET_POINT signal on conductor 25 and FRONT_SLOPE signal on conductor 33 in response to the STEP signal entered on input 34. The FRONT_SLOPE signal on conductor 33 occurs when the SIGN signal is present on conductor 26 and the SET_POINT signal on conductor 25 is increasing in response to the STEP signal on input 34 for one quarter of a cycle.

The PWM_OSC signal waveform 36 and the TEST signal waveform 37 are shown in Figure 2 as a function of time.

While the TEST signal is present on conductor 21, the bridge control logic 14 activates the switches S1-S4 in the H bridge via switch driver 15 and conductors 29-32 to cause the phase current to flow in the REV direction. At the PWM_OSC edge 36, the bridge control logic 14 switches to FWD phase current or continues to provide REV phase current depending on the FWD and REV signal levels. If REV signal is not present, the bridge control logic 14 activates the H bridge 16 for FWD phase current until FWD signal is present indicating the I_SENSE signal on conductor 23 has risen to the SET_POINT. Phase current will then RECIRC . If REV signal is present at the PWM_OSC edge 36, the phase current is above the SET_POINT and the bridge control logic 14 will maintain the REV phase current condition until the REV signal on conductor 28 ceases thereby indicating that the I-SENSE signal on conductor 23 has decreased to the SET_POINT. Phase current will then RECIRC.

During stationary and low speed motor operation, it is not generally required to remove excess phase current. However during high-speed motor operation when the SET_POINT is rapidly decreasing, back EMF causes the motor phase current to be above the SET_POINT requiring the active removal of phase current, as described earlier, for substantial improvement in current control operation. It is to be noted the other motor phases can use the same PWM-OSC edge or the other PWM-OSC edge.

The PWM oscillator 12 adjusts the frequency of the PWM_OSC signal on conductor 22 when there are fewer than a specified number of PWM_OSC edges present during the input of the FRONT_SLOPE signal to the PWM oscillator 12. If the PWM oscillator 12 counts less than the specified number of PWM_OSC edges during the occasion of the FRONT_SLOPE signal, the PWM oscillator 12 frequency is increased by a fixed amount when the FRONT_SLOPE signal ceases. This will occur during each FRONT_SLOPE signal occurrence until there are the minimum specified number of PWM_OSC edges present or the preset maximum frequency within the PWM oscillator is reached, whichever occurs first, to thereby maintain a minimum number of PWM_OSC edges during the quarter cycle while the motor is in operation or until the maximum operating frequency of the PWM oscillator 12 is achieved. It is to be noted that the counting of PWM_OSC edges to thereby accurately control the motor phase current during high-speed motion could be performed during any portion of the motor operating cycle

The max time logic 13 connects between the PWM oscillator 13 and the bridge control logic 14 to create a MAX_TIME signal on conductor 35 that occurs after the designated percentage of the PWM_OSC signal period has elapsed. The period timing begins with the edge of the PWM oscillator 36. . When MAX_TIME signal occurs, the bridge control logic 14 will discontinue either the FWD or REV phase current, if required, placing the H bridge into the RECIRC condition. While in the RECIRC condition, MAX-TIME has no effect during the TEST period 37. It is to be noted that the other motor phases can use the same PWM- OSC edge or the other PWM-OSC edge.